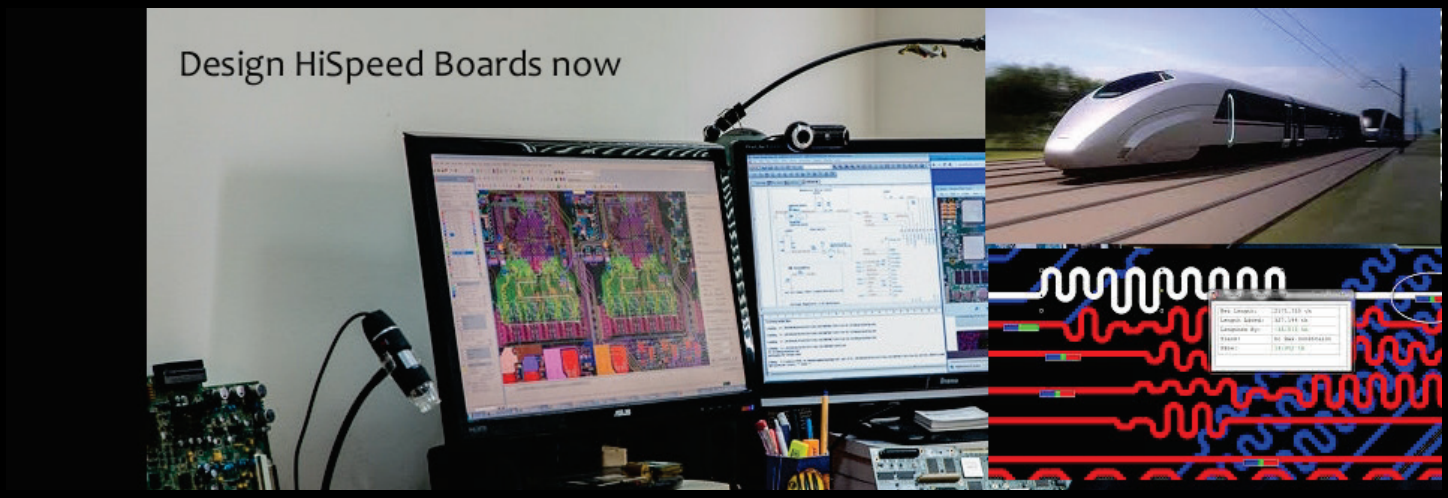
HI-Speed Designing with Altium Designer



Introduction

We are living in Digital & and Hi-Speed theory applies here. We might be knowing about Hi speed in bits and bytes, but may not know the correct methodology to implement during system design & its implementation on PCB Layout design. Further, knowing Hi-Speed & implementing through a particular EDA tool like Altium is a challenging task. CEDA-Labz has launched a unique approach towards implementation High speed design when you route boards in ALTIUM Designer.
This multimedia training gives the engineer and designer the fundamental knowledge necessary to make the most efficient design rule set for his or her high speed design, to organize the design process to most efficiently execute the design, to select the appropriate materials for the PCB itself, and to select the tool set that will make the design process most efficient.

Targeted Audience
Digital Logic Engineers, System Architects, EMC Specialists, Technicians, Engineering Managers, Project Managers, PCB Layout Professionals. Anyone, who works with High Speed Digital Logic. Anyone who works with any digital logic produced by the submicron processes currently becoming standard in the industry.

Benefits of this Course

As speeds of all logic families have increased, the importance of managing high speed effects in the interconnects of a system have become ever more important. Advances in semiconductor technologies have resulted in standard ICs with switching edges as fast as 300 Pico seconds. Coupled with this, system clock rates in excess of 500 MHz are becoming common. At the same time, designs have become more complex and time available to execute designs and correct design problems have decreased. This dual need to cope with ever increasing circuit speeds and ever decreasing design times has made it imperative for engineers and designers to become proficient in the skills and methods once only the province of super computers.

This drive for higher speed and higher performance products is resulting in a variety of high-speed design problems. **Some of these are:**
Failures related to lack of impedance and reflection control.
Failures from cross talk or coupling.
Problems related to time delays in PCB traces.

Failure to meet EMI specifications
Failures from inadequate or improper power supply decoupling or bypassing.
Due to the fact that most of these problems are related to the edge rates of the logic devices being used, every electronic product, even if it is intended for a "low speed" application, is a candidate for these failures when not designed with high-speed rules. This course will give the participants the tools and information required to recognize when a circuit has the potential for high-speed problems. The skills and techniques needed to set up design rules and a design process to insure these circuits function correctly when designed will also be covered.

Course Content : It has been divided into 2 sections - TECHNOLOGY & IMPLEMENTATION

TECHNOLOGY

VIDEO1
Defnitions
EMI
Understanding Cross Talk
Approach

VIDEO2 High Speed Guide -Courtesy Analog Devices

Overview
Schematic
Location
Trust no one
Power Supply bypassing
Parasitics
Ground and Power planes
Packaging
RF Signal routing and Shielding Checking the Layout
Summary
HiSpeed Tutorial_Ver2 -in pdf format

IMPLEMENTATION

Audio-Video on High speed design implementation on BOARD
Introduction
Defining Net Class and Differential pair
Defining Rules for Class and Differential pair
Length tunning
Defining Room and rules for the ROOM

OVERALL IT'S A SHORT COURSE BUT ENOUGH TO IMPLEMENT HISPEED ON BOARDS