

**PCBKEY**

ONLINE Signal Integrity & EMC Course -

**"RIGHT THE FIRST TIME" with HyperLynx®** 

SIGNAL INTEGRITY & EMC with Hyperlynx course on demand at your desk without leaving your workspace - **No-campus attendance No commuting No travel cost No deadline pressure.** Enroll any time and enjoy affordable fee.

**"RIGHT THE FIRST TIME" with HyperLynx®** is a Signal Integrity and Electromagnetic Compliance "how to do it right" class that gives students a well-rounded explanation of proper high-speed system design. The course is based on a design methodology developed by a major telecommunications company, which has been documented over multiple years and thousands of designs to produce "right the first time" results 99% of the time. "Right the first time" means the systems work correctly at full speed, they are reliable, they have clearly defined manufacturing margins, and they are quiet enough to pass FCC & CISPR radiated emissions tests... on the first try!

**Target Audience:** Engineers and CAD Layout Designers responsible for implementing high-speed digital and mixed analog digital systems that will work reliably at full speed and still remain quiet enough to pass regulatory EMI tests. The basic methodology upon which this class is based was documented to achieve repeatable first pass success as a standard practice.

### Why Should I attend this Training?

*Increasingly fast edge rates in today's integrated circuits (ICs) cause detrimental high-speed effects, even in PCB designs running at low operating frequencies. As driver ICs switch faster, a growing volume of boards suffers from signal degradation, including over/undershoot, ringing, glitching, crosstalk, and timing problems. When degradation becomes serious enough, the logic on a board can fail.*

**Any Electrical Engineer, CAD Layout Designer, or Technical Manager** tired of design which works now and which do not works after some time, 2 out of 10 board works can get a nightmare whether the next lot of production run is going to work or whether its going to pass FCC & CISPR compliance test would find this class extremely useful. Students who have implemented this methodology have regularly produced complex designs that do indeed work correctly on the first implementation. On average, that saves about \$10000 and two months on the average system using 2006 technology. Any financially responsible manager will agree that saving two designs turns on the typical system results in huge savings and potentially even larger profits by getting to market earlier.

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Updated January 11, 2014

# Right The First Time – Part I

“RIGHT THE FIRST TIME” with HyperLynx<sup>®</sup> is delivered in 2 Parts, Part I and Part II

## PART-I Content

**Basic Signal Integrity** including board layer stack-up specification, high-speed routing topology, space, trace, termination practices, and return current control. Get this wrong and the system will reward you with a host of problems including False Clock, False Data, Negative Timing Margins, Clock Jitter, Excessive EMI as well as a host of Manufacturing and Reliability issues.

**Power Delivery** is a lot more than one 0.1uF and five 0.01uF caps per pin. Power delivery depends upon stack-up, capacitor selection, placement, mounting technique, and quantity. Typical target impedance for memory systems must be around 0.1 ohm from DC to the highest frequency of interest. The highest frequency of interest is most likely in the microwave region. Poor design can result in power delivery impedance poles and inter plane resonance. Many of the mysterious SI and EMI issues can be traced directly to poor power delivery design.

**Root causes and cures for EMI.** The class’s primary approach is to stop the noise at the source. If noise is eliminated at the source, you do not need to chase it around the board. The recent proliferation of ASIC’s from hell has prompted us to add a section on shielding and filtering. If the problem is in the device, not the board, and you can not find a better behaved substitute for that device, your only choice is to shield and filter.

**Single Ended Bus Issues.** If you have a memory or address bus with both high and low speed devices, do the high speed devices belong close to the processor with the low speed devices farther away, or vice versa? How do you terminate? What about option slots?

**How LVDS really works.** With the huge noise margin available using LVDS devices, you can use almost any interconnect scheme. However there can be other complications like Cross Talk and EMI if you do it incorrectly.

**Giga Bit Serial / SERDES interface routing issues ...PCI Express** We explain what is important and also debunk some of the popular myths about routing these types of interfaces.

**The Analog / Digital Interface** i.e. Isolation vs. Communication

**Understanding** the issues related to “quiet grounds.”

**Connectors,** Board-to-Board SI, EMI, and Power Issues

**Chip Level Package Issues** and how to defend against them.

**Basic Shielding Theory** as it applies to Switching Power Supplies

**Critical elements in an effective high-speed system design process.** Simply performing a solid pre-layout design review and including the correct personnel can raise your first time odds of success at least 50%. Implementing a full process can result in first time success 99% of the time.

## **Teaching Method ... Explain, Demonstrate, Do**

The instructor will **explain** the problem and an appropriate method to solve that problem. – **Audio & Slides Presentation**

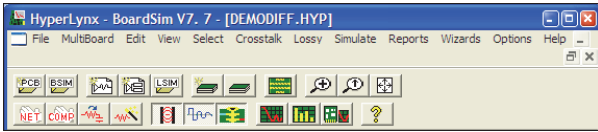
The instructor will **demonstrate** the solution using industry standard software tools. – **Audio Video Demonstration**

The students will **do** the work for themselves using lab computers and sample problems.

The students perform computer-based labs to help lock in understanding of the physics behind classical high-speed design problems. This also gives them the freedom to try their own examples. Simply hearing information results in about a 30% retention rate. Seeing a demonstration will raise the retention rate closer 50%. If you actually do the work on something meaningful to the student, the retention is over 80%.

The purpose of this class is not to get into complex formulae and higher math. There are perfectly good simulators to do the heavy lifting. The purpose is to give layout designers and EE’s the tools to make their next design a quiet, reliable, full speed system on the first try.

# HyperLynx® SI *continued* Part II

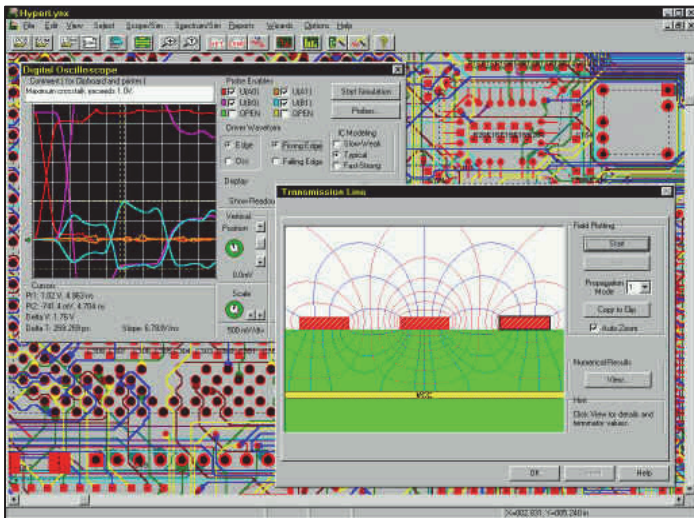


## You will learn how to

- Create and simulate LineSim cell-based and free-form schematics
- Investigate termination strategies
- Investigate stack-up strategies
- Translate design databases
- Identify and debug SI and Crosstalk issues
- Read eye diagrams and how to specify a mask
- Simulate EMC and evaluate the results
- Assign models and component values
- Evaluate SI and Crosstalk issues
- Translate PCB layout databases
- Run BoardSim simulations interactively and in batch mode
- Run BoardSim for both single and multi-board projects
- Evaluate batch mode simulation reports to identify potential problems

## Prerequisites

- Familiarity with High-speed PCB concepts



## The course kit comes with

1. HyperLynx Software evaluation CD
  2. Printed Training Manual
  3. MULTIMEDIA DVD with audio- video Classroom tutorial just like Live session
  4. Hyperlynx reference design and LAB session files
- Verified Certificate of Participation optional

**satisfaction-guaranteed**

Course Part# **PCBkeySI0709**

Pricing USD265 / INR 16427

## **PART-II Content**

**NOTE:** All lessons are documented with relevant Screenshots and Audio-Video demonstration which becomes much easier to kick start Hyperlynx & jump on a particular feature to make your learning interesting & easy

How LineSim Works

Simulating a Simple Clock Net In LineSim

Fixing the Clock Net 6

A Series-Terminated Net with IBIS Model

EMC Analysis of the Clock Net & Terminated Clock Net

About LineSim's Free-Form Schematic Editor

Signal-Integrity of a DDR Data Path

About Modeling ICs

How LineSim's Crosstalk Analysis Works

Differential-Signal Analysis

Crosstalk Exp: Planning Minimum Trace Separation on a Bus

Differential-Trace Example

Achieving a Specific Differential Impedance

LineSim's GHz Features

Lossy Simulations

Viewing Loss in the Frequency Domain

Integrated SPICE Simulations

Touchstone (S-Parameter) Modeling

Eye Diagrams and Multi-Bit Stimulus USB 2.0 Example

Modeling a PCB Stackup

Introduction

Overview of the Stackup Editor

How to Do Impedance Planning

Impedance Planning for Differential Pairs

HyperLynx Demonstration Post-Layout (BoardSim)

Post-Layout Analysis: BoardSim and Batch Mode

Introduction

How BoardSim Works

Translating your Board into BoardSim's Format

Batch Analysis of the Entire Board for Signal-Integrity, Crosstalk, and EMC Problems

Detailed Batch Analysis of Critical Nets

BoardSim's Crosstalk and Differential-Signal Features

How BoardSim's Crosstalk Analysis Works

Using BoardSim Crosstalk for Differential-Signal Analysis

Quick Analysis: Generating a Crosstalk Strength Report for an Entire PCB

Running Detailed Batch-Mode Crosstalk Simulations

BoardSim's GHz Features

Advanced Via Modeling

Visualizing a Via's Geometric/Electrical Characteristics

BoardSim's MultiBoard Feature

Quick-Start

Using Hyperlynx for Post PCB layout Simulation

HyperLynx - New Features and Enhancements

Background Information on Signal-Integrity, Crosstalk, EMC,

Hyperlynx and GHz Analysis

PCB Design Analysis Software Guidelines

HyperLynx Applications

Input Guidelines for HyperLynx BoardSim

HyperLynx Input/Output File Types

Modeling ICs / Why IC Models are Important

IC Modeling with HyperLynx

Conclusion

**Disclaimer:** Due to CEDA's policy of continuous improvement, specific course change without notice. Therefore, this agenda should be taken as a guide only part of any agreement between CEDA and any other party

# Multimedia Demonstrations

## Section One: Pre-Layout Analysis

### Chapter1:

#### Designing a Well Behaved Simple Clock Net

Clock nets must be short of properly terminated to avoid excessive ringing. One consequence of ringing is "input ring-back". This is when a signal fails to smoothly transition between the input threshold voltages of a receiver. It can result in false switching, meta-stable conditions and timing jitter. A schematic for a simple clock net is created and analyzed. The ring-back is quantified and parallel termination applied to eliminate.

### Chapter2:

#### Driver Strength and Overshoot Control

A second consequence of ringing is overshoot. This is when a signal swings past the supply or ground voltage. Excessive overshoot may saturate input transistors, slowing their switching time. In extreme cases it may even permanent damage ICs. A schematic for a second simple clock net is created using an IBIS driver model. The level of overshoot is measured using the typical, fast and slow driver characteristics. Series termination is applied to reduce overshoot.

### Chapter3:

#### The HyperLynx Termination Wizard

In the previous chapters a trial and error approach was used to choose termination values. In this chapter the HyperLynx Termination Wizard will be used to pick the optimal values for terminators.

### Chapter4:

#### Parameter Sweeping

Simulation with parameter sweeping allows you to study the effects of varying design property values. Passive and active component values can be swept, as can PCB geometric values. Sweeping can be used to optimize component values, do sensitivity analysis as well as solution space and reliability analysis. In this chapter a parameter sweeping will be applied to a series terminated net to determine the effect of changing driver strength and termination values.

### Chapter5:

#### Reducing EMC

HyperLynx supports two types of EMC analysis: spectrum analysis from current probes and prediction of the far field radiation at a specified point in space. Early detection of major EMC sources using current probes can avoid expensive redesign. In this chapter pre-layout EMC analysis will be demonstrated using a current probe on a net without adequate termination. The termination will be improved and the reduction in EMC.

### Chapter6:

#### Analyzing a more complex net: a simple DDR memory example

The examples used in previous chapters were simplified. In this chapter a net that is more typical of real world designs is analyzed. A DDR strobe net is simulated and waveform errors identified. The termination and trace lengths are then optimized to correct the waveform errors.

### Chapter7:

#### Designing a Multi-Gbps High Speed Serial Channel

High-speed serial channels require more complex signal integrity analysis. In this chapter it will be demonstrated that in the HyperLynx world, more complex does not mean more difficult to use. The chapter starts with the skeleton of a multi-Gbps example net. SPICE driver and load models will be assigned, as will accurate lossy-coupled trace models. The net will then be analyzed using HyperLynx FastEye which offers accelerated statistical and linear channel analysis. The eye opening and BER bathtub curves will be developed for the net with and without transmitter de-emphasis.

## Section Two: Post-Layout Analysis

### Chapter8:

#### Interactively Validating a Clock Net after Placement and Routing

Previous chapters have concentrated on pre-layout analysis. Fixing signal integrity problems early in the design process will provide enormous payback in the minimizing the cost of redesign and lost market opportunity. Even so, compromised are always present in the process of PCB layout and routing, so it is critical that post-layout signal integrity validation be conducted. In this chapter, interactive post-layout analysis will be used to identify a termination issue. The HyperLynx Termination wizard will be used to correct the problem.

### Chapter9:

#### Interactive Crosstalk Analysis

Nets on high-density printed circuit boards will be subject to crosstalk from adjacent nets. In this chapter, an example net will be analyzed to establish which adjacent nets inject into it a significant crosstalk voltage. A crosstalk threshold voltage will be set in HyperLynx, so it can automatically extract the circuit for a net together with its neighboring nets to which it has strong coupling. The circuit will then be simulated to quantify the level of crosstalk.

## Section Three: Additional Topics

### Chapter10:

#### PCB Layer Stack-up Editing and Trace Impedance Planning

Creating a good PCB layer stack-up is essential to meet the mechanical, signal and power integrity demands of a design. Trace impedance must be controlled to minimize reflections. Reliable return paths must be provided for signaling currents. Crosstalk must be limited. In addition, there must be adequate power distribution. In this chapter an example PCB layer stack-up will be created. Some of the critical elements of stack-up design will be discussed. Finally trace impedance planning will be done for single ended and differential nets.

Learn the skills you need to succeed as a PCB SI Engineer  
- at home, workplace at your own pace.

# PCBKEY

KEY to your ONLINE PCB DESIGN & SIGNAL INTEGRITY TRAINING needs



**E /DISTANCE LEARNING**

Keeping your design skills up to date requires continually learning and exploring the latest tools, techniques, and methodologies. However, it can be hard to fit training and travel time into busy project schedules. **PCBkey** offers Online training as a flexible and cost-effective alternative to site-based training. PCBkey Training is a part of CEDA located at New Delhi, INDIA.

## About Online/Distance Certificate course

Online Training is a Virtual Classroom audio-video environment that allows you to feel in live training events without the need to travel. You listen to lectures, participate in lab exercises, ask questions, and receive feedback just as you would do in a conventional classroom— except you do it from the **convenience of your desktop**, or anywhere you have an Internet and phone connection. It saves the hassle, expense, and travel time to a training site.

## Why choose Online/Distance course?

**Save 75%** training cost to improve your productivity by learning the very latest tools.

Virtual classes consist of multiple three-hour sessions spread over several days, leaving the rest of each day free for you to concentrate on your design projects.

## What I need at my end?

A Windows based PC preferably with Internet connection or a Phone

## Who will be benefited?

Fresh engineering graduates, Instructors, design engineers, new Board Designers, Embedded designers, project executives, project leaders, PCB Designers, High-SPEED Designers, Signal Integrity Engineers.

## What is **inside** the Courseware?

1. Hyperlynx Software
2. Printed Training-Manual
3. MULTIMEDIA DVD with audio- video Classroom tutorial just likes live session.
4. Example files for reference
5. Certificate after project completion.
6. Right the First Time – Practical Handbook on Signal integrity by LEE.W.RITCHEY – 639 pages in PDF Format



Course Material

## How it works? How I practice? What is the support level?

Install the HyperLynx Software package from the **DVD** inside the course material.

Training consists of conventional written discussions (in Adobe Acrobat®) of subjects, including links to multimedia demonstrations.



A click on the **"Show me now"** opens an audio-video clip showing exactly how to perform a specific action. User controls are available to pause or repeat the clip until the action is understood. Additionally, the same files used to create the demonstrations are included, allowing further practice for LAB session

Practice the LAB session on your own – WERE STUCK? A Click on the **"Show me now"** opens an audio-video clip showing exactly how to perform a specific action. **...Still not clear?** Phone or email us – Your Specialized Tutor will be happy to help you. At this end **almost 24x7**, one-specialist tutor will be present to **support** - clarify your doubts through either email or phone.

## Feedback

"The course provided me with a better understanding of why a board design fails to pass EMC compliance and will assist in resolving failures. Also, we feel now we are one step ahead of anyone who has not attended this Training. It's a good effort to put all relevant issues of SI in one".

*Vinod Sharma, Max Remmer - Samsung*

*Dr. M. Narayanan – American University of Sharjah*  
*Victor Naobia – Nigerian College of Aviation Technology, Zaria*



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