VLSI Design *Distance Learning*

Course Part# PCBkeyVLSI0214

CEDA-Labz

CEDA-Labz VLSI Distance learning Courseware is packed with all necessary Hardware, Software, Cables and Hardware is a complete Courseware – You need not to download or buy anything to start the Course, designed by Verilog Designers and Academicians from Digital and VSLI Domain with experience more than 10 years

Learning Objectives

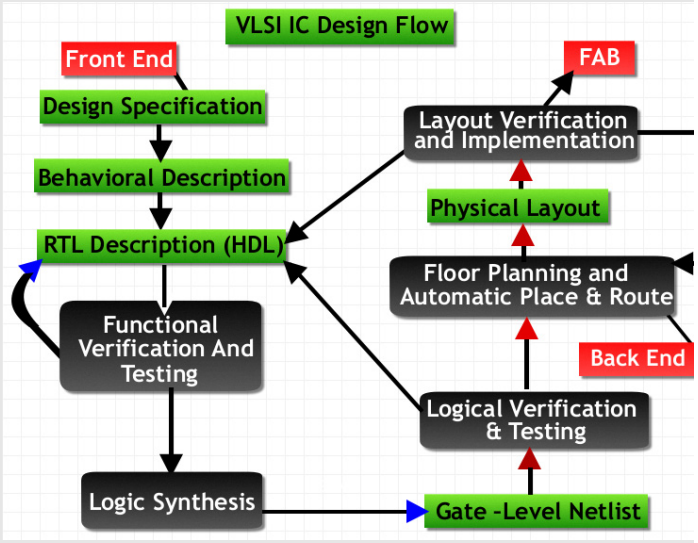
Learn the skills you need to succeed as a VLSI design engineer - at home, at your own pace. Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip.

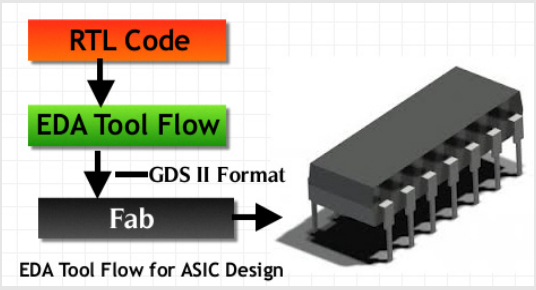
VLSI Design training is based on FPGA design flow with Xilinx tools. This program will help you to design Complex digital systems using Verilog and to get experience of Processor and controller implementations on FPGAs.

Training modules start with solid basics. You will begin by learning the important principles that are the fundamental rules for just about, whatever you may do in VLSI design. Then, you will get detailed instruction in techniques and procedures. Step by step, we'll guide you through exciting hands-on projects like Processor implementation on FPGA that you can complete in your PC anywhere

Courseware Includes

- Audio-Video Session in USB Pen drive
- VLSI Board – Xilinx Spartan based
- Cable for Xilinx Board and PCB Connectivity
- ModelSim Timing Simulation Software
- Xilinx ISE Software
- Verilog Example codes
- User Manual Hard copy
- VLSI Board Schematics, Data Sheet





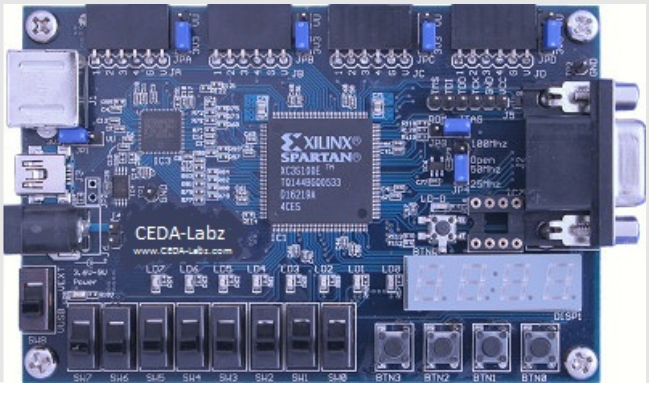
EDA Tool Flow for ASIC Design

Board Features:

- 100,000 gate Xilinx Spartan 3E FPGA
- JTAG programming port
- XCF04S Xilinx Platform Flash ROM to store FPGA configurations
- Large collection of I/Os including eight LED's and four slide switches
- LCD and 7 segment displays
- RS 232 and VGA ports
- Ethernet port with physical layer controller
- User-selectable oscillator, plus a socket for a second oscillator
- 100 pin user I/O and peripheral module connection

FPGA Features:

- 100k gates.
- 108 I/Os.
- 72k Block RAM.
- 15k Distributed RAM.
- 240 CLBs.



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Audio Video Session

1. Introduction to Integrated Circuit Technology

- Evolution of ICs
- Evolution Of Computer-Aided Digital Design
- Design Flow For Designing IC
- Chip Fabrication and MOS Technology
- Chip manufacturing processes
- VLSI products
- Scope of VLSI – different Domains and Fields
- Challenges and trends – power, speed and area

2. Verilog HDL

- **Introduction to HDL**
  - Need of HDL
  - Advantages of HDL
  - Types of HDL
- Design methodologies
- Verilog Program structure
  - Module
  - Instance
  - Ports
- Data Types
- Parameters
- System Tasks And Compiler Directives
- Simulation
  - Design Block
  - Stimulus Block
- **Different Style of modeling**
  - Gate Level Modeling
  - Data Flow Modeling
  - Behavioral Modeling
  - Switch level Modeling
- **Gate level Modeling**
  - Basic Primitive gates
    - Single Input-Multiple Output
    - Multiple Input-Single Output
    - Tri-state Gates
  - Gate delays
  - Some examples
- **Data Flow Modeling**
  - Operators in Verilog
    - Arithmetic Operator
    - Relational Operator
    - Equality Operator
    - Logical Operator
    - Bitwise Operator
    - Reduction Operator
    - Shift Operator
    - Conditional Operator
    - Concatenation Operator
    - Replication Operator
- Continuous Assignment Statement
  - Syntax
  - Implicit Continuous Assignment Statement
  - Some examples
- Delays in data flow modeling and Examples
- **Behavioral Modeling**
  - Structured Procedure Assignment
    - Initial
    - Always
  - Difference between them
- Procedural Assignment Statements
  - Syntax
  - Some examples
  - Types of Procedural Assignment Statements
    - Blocking statements
  - Non-blocking Statements
- Timing Control Statements
  - Delay based
  - Event Based
    - Edge Triggered
    - Level sensitive
- Block Statements
  - Sequential
  - Parallel
- Delays in Behavioral Modeling
  - Inter-statement
  - Intra-statement
- Conditional Statements
  - If-else
    - Syntax
    - Some examples
  - Case
    - Syntax
    - Some examples
- Loop In Verilog
  - for
  - while
  - forever
  - repeat
- **Examples of Combinational & Sequential design using Verilog**
- **Asynchronous and Synchronous Reset Design Examples**
- **State Machine Design Example**
  - Mealy Machine Design
  - Moore Machine Design
- **Task and Function**
- **Delay Models In Verilog**
  - Distributed Delay
  - Lumped Delay
  - Pin-to-pin
- **Switch Level Modeling**
  - Syntax
  - Some examples
- **User Defined Primitives**
  - Rules For UDP Writing
  - Some Examples

3. How to Use Modelsim for Design HDL and Simulation

- Basic designs modeling using Modelsim
  - Basic Combinational Design
  - Basic Sequential Design
- Compiling the design
- Simulation of Design using Modelsim

4. Programmable devices

- Programmable Logic & Technologies
  - ASIC
  - Types & Advatages
- Purpose of PLD's
- Programmable IC
  - SPLD
  - ROM
  - PLA
  - PAL
- CPLD's
  - Why CPLD
  - What is CPLD
  - CPLD Structure and Design
  - CPLD Manufacturer's
  - Advantages
- FPGA Architecture

5. FPGA Design Flow

- Steps in Design Flow
- FPGA Device Programming

6. How to make and implement a Design Using Xilinx ISE

- Basic Gates
- Basic Combinational Logic
- Basic Sequential Logic